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<u>L49</u>	(712/26,26, 216,217)![CCLS]	68	<u>L49</u>
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<u>L46</u>	130 and 134	126	<u>L46</u>
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<u>L41</u>	132 and 135	5	<u>L41</u>
<u>L40</u>	132 and 134	90	<u>L40</u>
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Freeform Search Page 2 of 3

<u>L38</u>	133 and 135	0	<u>L38</u>
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<u>L32</u>	L30 and (allocat\$5 or assign\$7) and microprocessor\$1	586	<u>L32</u>
<u>L31</u>	L30 near45 (allocat\$5 or assign\$7)	48	<u>L31</u>
<u>L30</u>	(pseudo or random\$3 near4 generat\$4) near15 decod\$4	3645	<u>L30</u>
<u>L29</u>	L28 near25 microprocessor	17	<u>L29</u>
<u>L28</u>	(random\$3 near4 generat\$4) near15 decod\$4	1601	<u>L28</u>
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<u>L23</u>	L22 and 19	36	<u>L23</u>
<u>L22</u>	(simd or single near1 instruction) and 17	43	<u>L22</u>
<u>L21</u>	17 and 111	4	<u>L21</u>
<u>L20</u>	17 and 110	17	<u>L20</u>
<u>L19</u>	17 and 19	43	<u>L19</u>
<u>L18</u>	112 and 111	4	<u>L18</u>
<u>L17</u>	112 and 110	17	<u>L17</u>
<u>L16</u>	112 and 19	41	<u>L16</u>
<u>L15</u>	17 and 111	4	<u>L15</u>
<u>L14</u>	17 and 110	17	<u>L14</u>
<u>L13</u>	17 and 19	43	<u>L13</u>
<u>L12</u>	independent\$5 and 17	74	<u>L12</u>
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<u>L11</u>	(712/3)[CCLS]	56	<u>L11</u>
<u>L10</u>	(712/2-15,221,224)[CCLS]	1758	<u>L10</u>
<u>L9</u>	(712/2-300)[CCLS]	11997	<u>L9</u>
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<u>L8</u>	L7 and 16	13	<u>L8</u>
<u>L7</u>	interlock\$5 and scalar near15 vector	95	<u>L7</u>
<u>L6</u>	(one or single) near5 (clock or cycle) near10 (issu\$5 or send\$3 or sent or transfer\$5)	19175	<u>L6</u>
<u>L5</u>	interlock\$5 near15 scalar near15 vector	9	<u>L5</u>
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<u>L4</u>	L3 and (cycle or clock)	1	<u>L4</u>

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Page 3 of 3

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